In Micro-electronics it's GMe

MOS MONOLITHIC 100-BIT SHIFT REGISTER

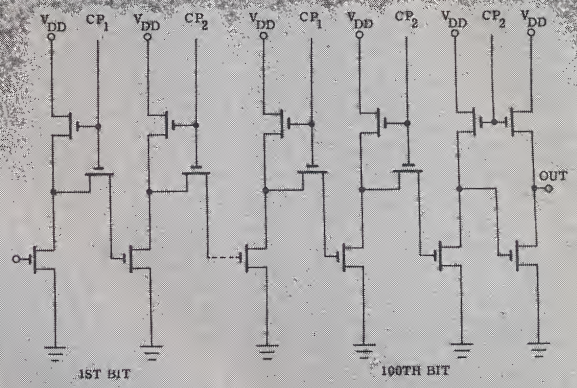
pL 5100

JULY 1965

The GMe pL5100 MOS Monolithic 100-Bit Shift Register was designed for use in two-phase clocked sequential digital systems. The pL5100 provides a maximum amount of storage in a single TO-5 can and can be cascaded to provide longer delays or larger capacity memories. Some of its outstanding features are:

- **Low power consumption — 2 mw/bit**
- **Clock rate — > 2 Mc**
- **Full mil temperature range — −55°C to +125°C**

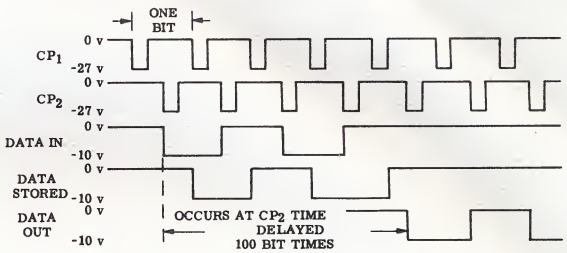
This system can be interfaced with RTL circuitry as shown in the Applications. A simple two-phase clock generator is also shown in the Applications.



ABSOLUTE MAXIMUM RATINGS

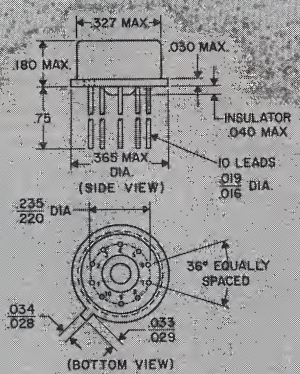
Voltage applied $V_{1,2,3,4,6,7,9}$ (Note 1)	- 35 v
Storage temperature range, ambient	- 55°C to +150°C
Operating temperature range	- 55°C to +125°C

TYPICAL TIMING DIAGRAM

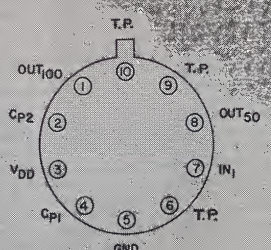


PACKAGING

Low profile TO-5 package



PIN CONFIGURATION



Pins 6, 9, and 10 are test pins and must be grounded for normal operation.

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ELECTRICAL TEST SPECIFICATIONS (Notes 2, 3, 5, 6)

Standard conditions:

T_A = +25°C, V_{DD} = -20 v, Load = 10 meg and 7 pf, CP_1 and CP_2 = -27 v

Input word used for measurements = 010011000111

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Repetition Rate	10			kc	CP_2 = 1 μsec CP_1 = 0.5 μsec
Clock Repetition Rate			1.0	Mc	CP_2 = 0.5 μsec CP_1 = 0.3 μsec
Power Consumption		2.5	3.5	mw/bit	Pulse Rep. Rate = 1 Mc/sec CP_2 = 0.5 μsec CP_1 = 0.3 μsec
Power Consumption		0.024	0.10	mw/bit	Pulse Rep. Rate = 10 kc/sec CP_2 = 1 μsec CP_1 = 0.5 μsec
Input Data Logic "0"			-4.0	volts	CP_2 = 0.5 μsec
Input Data Logic "1"	-8.0			volts	CP_1 = 0.3 μsec
Output Data Logic "0"			-3.0	volts	CP_2 = 0.5 μsec
Output Data Logic "1"	-9.0			volts	CP_1 = 0.3 μsec
AC Noise Immunity Logic "0" and Logic "1"	1.0			volt	Note 4 CP_2 = 0.5 μsec CP_1 = 0.3 μsec

NOTES

1 Voltage subscripts refer to pin numbers. Pins not specifically referenced are left electrically open.

2 All voltage measurements are referenced to pin 5.

3 Exercise caution to insure that the V_{DD} supply does not exceed +0.3 v when set to zero, as is the case for some supplies; otherwise the positive voltage will forward-bias drain-to-body junctions and destroy the devices.

4 AC noise immunity is defined as follows:
"1" state N. I. = $V_{1\ MIN} - V_{1\ TH} = |-9\ v| - |-8\ v| = 1\ v$
"0" state N. I. = $V_{0\ TH} - V_{0\ MAX} = |-4\ v| - |-3\ v| = 1v$

5 Units are 100% tested to this specification but these conditions do not represent the optimum limits.

6 Manufacturer reserves the right to make design and process improvements.

7 This shift register can be selected to operate with V_{DD} -12 volts and $CP_1 = CP_2$ = -24 volts.

The GMe pL5100 Shift Register can be used in a large number of applications where its large storage capacity would be advantageous. A few of these applications are:

- A FREQUENCY DIVIDER. Add one inverter in a closed loop and the frequency is divided by 2N where N is the bit length of the register.
- A MEMORY REGISTER. By tying the register back on itself and recirculating, the register will hold a digital word or pattern of pulses indefinitely. An example of this scheme is shown below. (Fig. 1)

Fig. 1 A possible approach to recirculate data in the register and store new data as required.

- A FIXED OR VARIABLE DELAY LINE where the length of the register is directly related to the clock frequency as shown in the schematic below.
- A REGISTER IN A DDA. The register can easily be integrated with the necessary logic to make functional blocks for a DDA.

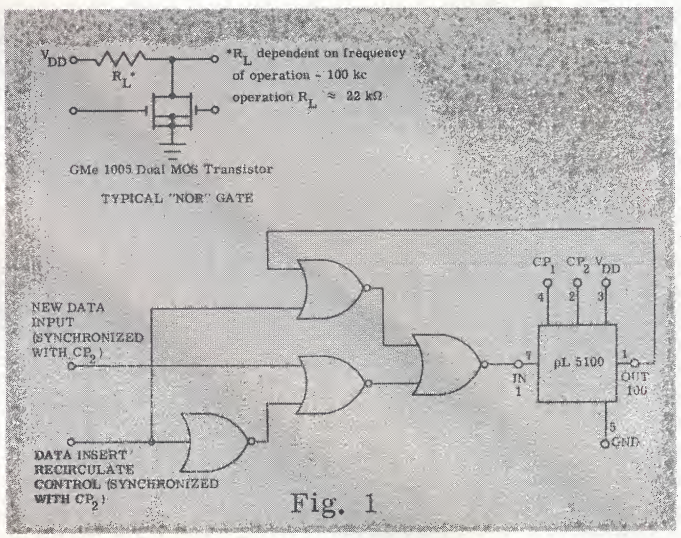


Fig. 1

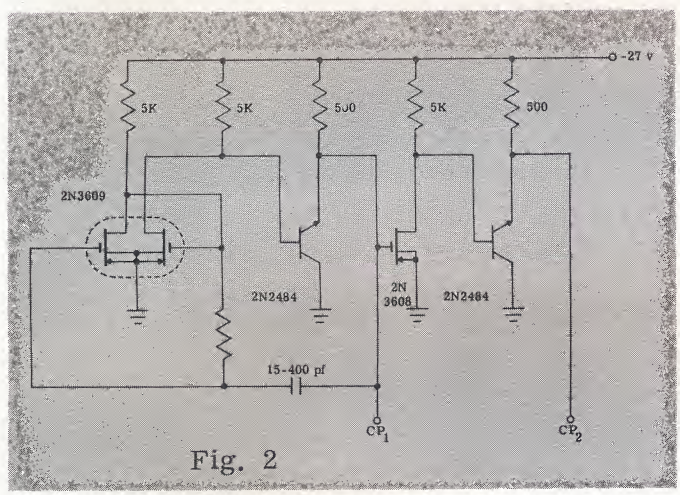


Fig. 2

Fig. 2 A clock generator which can be easily built out of MOS devices and NPN transistors. The size of the capacitor will determine the operating frequency. This clock generator provides opposite phase 50% duty cycle clocks. For minimum power dissipation, smaller duty cycles should be used.

Fig. 3 In order for the pL5100 to be used with standard NPN transistor logic, a buffer stage will be needed. One configuration, using a PNP transistor to interface RTL, is shown. A similar approach can be used to interface DTL.

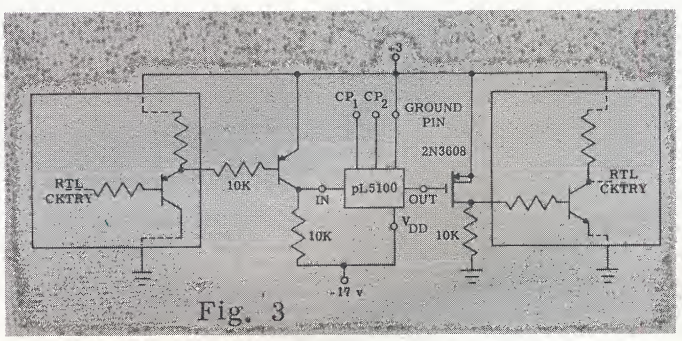
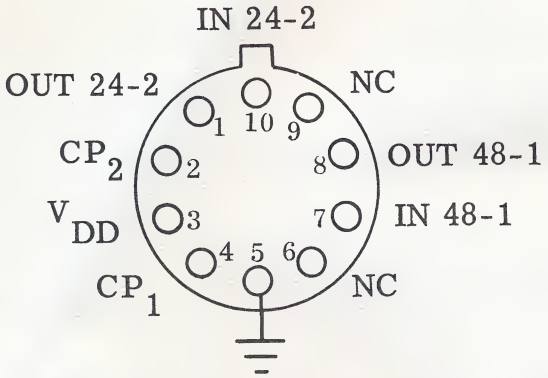
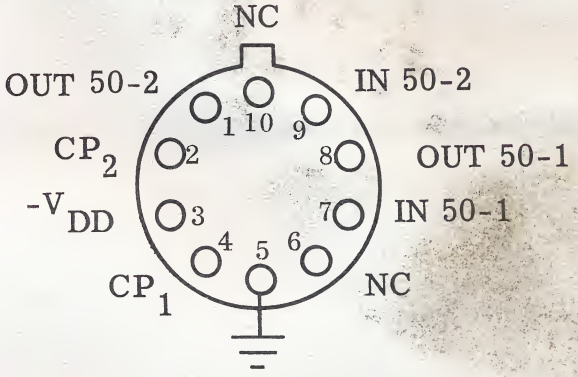


Fig. 3

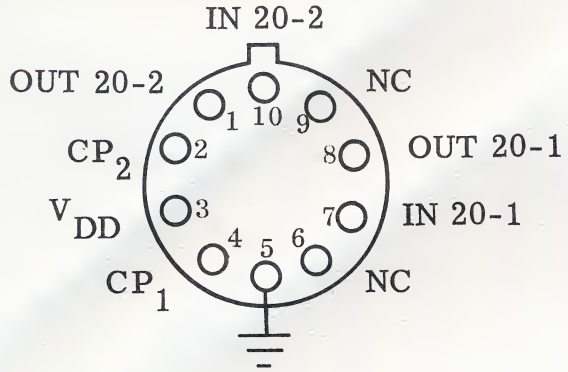
Additional GMe Dynamic Shift Registers. The electrical specifications for the pL5100 apply to the following registers:



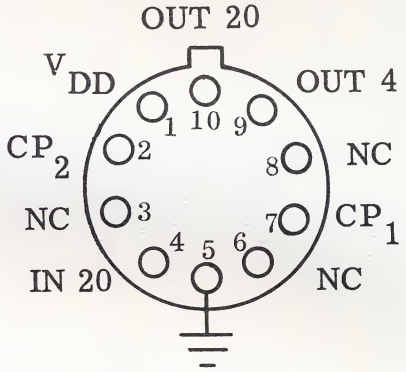
Top View 10 Lead TO-5
pL 5172 24 AND 48-BIT REGISTER



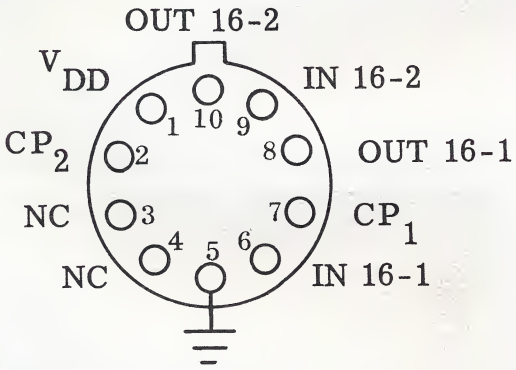
Top View 10 Lead TO-5
pL 5150 DUAL 50-BIT REGISTER



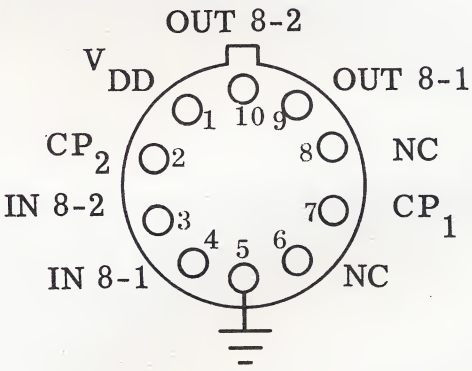
Top View 10 Lead TO-5
pL 5120 DUAL 20-BIT REGISTER



Top View 10 Lead TO-5
pL 5220 20-BIT REGISTER



Top View 10 Lead TO-5
pL 5216 DUAL 16-BIT REGISTER



Top View 10 Lead TO-5
pL 5208 DUAL 8-BIT REGISTER

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TECHNICAL DATA SHEET • TENTATIVE SPECIFICATIONS

9-BIT SHIFT REGISTER PARALLEL OUT

pL 4R02

SEPTEMBER 1965

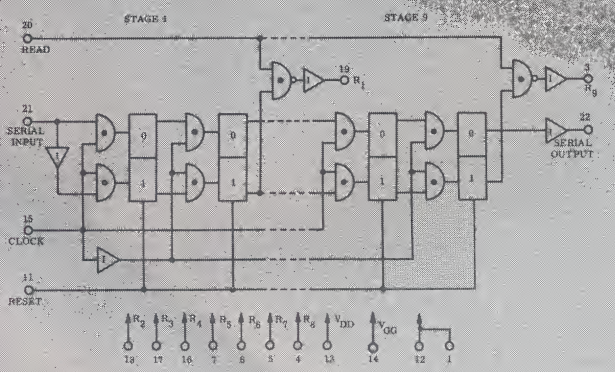
FUNCTION:

The GMe pL4R02, a monolithic integrated circuit using MOS devices, is a nine-stage shift register with gate-controlled buffered outputs from each register stage. This unit will operate from dc to 100 kc. The pL4R02 is useful as a serial-to-parallel converter, a sequencer or an arithmetic accumulator register.

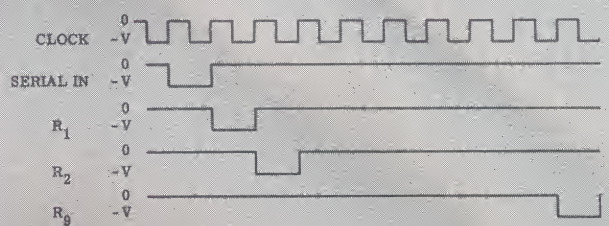
OPERATION:

The pL4R02 consists of nine master-slave flip-flops connected as a shift register. The master-slave flip-flops require a complete clock cycle to accomplish a one-bit shift. All inputs are buffered and inverted where necessary, requiring only single-line inputs. A negative clock signal (logic "1") shifts data into the master flip-flop and a ground signal (logic "0") shifts data from the master to the slave flip-flop. The reset and read commands are actuated by a logic "1" input. The reset signal is directly applied to both the master and slave flip-flops of all stages of the register. The ninth stage of the register has two true outputs available. The serial output is not gated and is continuously available. A typical operation of the pL4R02 is shown in the Timing Diagram.

FUNCTIONAL BLOCK DIAGRAM

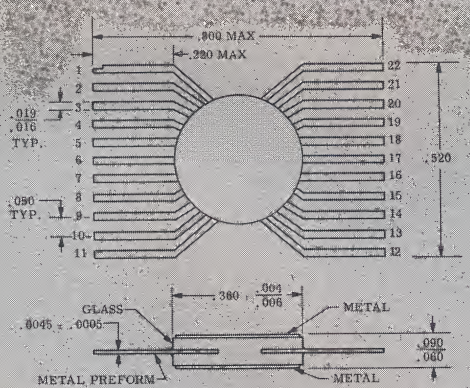


TYPICAL TIMING DIAGRAM



NOTE: READ COMMAND > -9V
RESET COMMAND < -3V

PACKAGING



Pin No.	Description	Pin No.	Description
1	Ground	12	Ground
2	N.C.	13	Power Supply (V_{DD})
3	9th Read Output (R_9)	14	Power Supply (V_{GG})
4	8th Read Output (R_8)	15	Clock Input
5	7th Read Output (R_7)	16	4th Read Output (R_4)
6	6th Read Output (R_6)	17	3rd Read Output (R_3)
7	5th Read Output (R_5)	18	2nd Read Output (R_2)
8	N.C.	19	1st Read Output (R_1)
9	N.C.	20	Read Input
10	N.C.	21	Serial In (S_{in})
11	Reset	22	Serial Out (S_{out})

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ELECTRICAL CHARACTERISTICS

Standard Conditions: (Unless otherwise noted)

T_A = -20°C to +70°C, V_{DD} = -12 v, V_{GG} = -24 v, Load = 10 MΩ and 7.5 pf.

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock-Pulse Repetition Rate	dc		100	kc	Pulse Width = 5.0 μsec
Clock-Pulse Rise and Fall Time			10.0	μsec	Pulse Width = 100 μsec, f = 1 kc
Input Pulse Width	1.0			μsec	
Input Logic Levels (Note 1)					
Logic "0" (V_{0TH})	0		-3.0	Volts	dc
Logic "1" (V_{1TH})	-9.0		-12.0	Volts	
Output Logic Levels					
Logic "0" (V_{0MAX})		0.5	-2.0	Volts	dc
Logic "1" (V_{1MIN})	-10.0	11.0	-12.0	Volts	
DC Noise Immunity (Note 3)					
Logic "0" and Logic "1"	1.0			Volt	
Input Capacity		3.0		pf	V_{IN} = 0 v
Input Leakage Current			1.0	μa	V_{IN} = -10 v
Output Impedance to Ground (Output Logic "0")		1000	2000	Ohms	
Short-Circuit Output Current	400			μa	
Turn-off Time (T_{OFF}) (Note 2)		1.5	2.0	μsec	Input Logic Levels "0" = -2 v, "1" = -10 v
Turn-on Time (T_{ON}) (Note 2)		0.1	0.5	μsec	Input Logic Levels "0" = -2 v, "1" = -10 v

NOTES

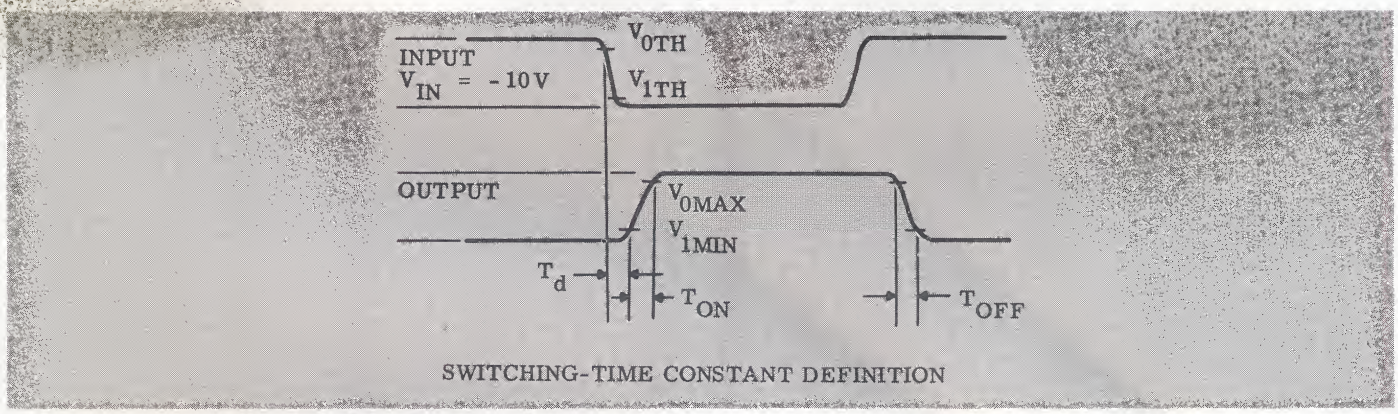
1. The input logic levels apply to serial input, read, reset, and clock inputs.
2. Turn-on and turn-off times are defined as logic level changes.
3. DC noise immunity is defined as follows:

$$\text{"1" State N.I.} = V_{1\,MIN} - V_{1\,TH} = |-10| - |-9| = 1\text{ v}$$
$$\text{"0" State N.I.} = V_{0\,TH} - V_{0\,MAX} = |-3| - |-2| = 1\text{ v}$$

4. Exercise caution to insure that the power supplies and input signals do not exceed +0.3 volts; otherwise, the PN junction used for gate protection will be forward-biased and damage may result.
5. Manufacturer reserves the right to make design and process improvements.
6. The bias voltages of V_{DD} = -12 v and V_{GG} = -24 v were selected for -20°C to +70°C operation.

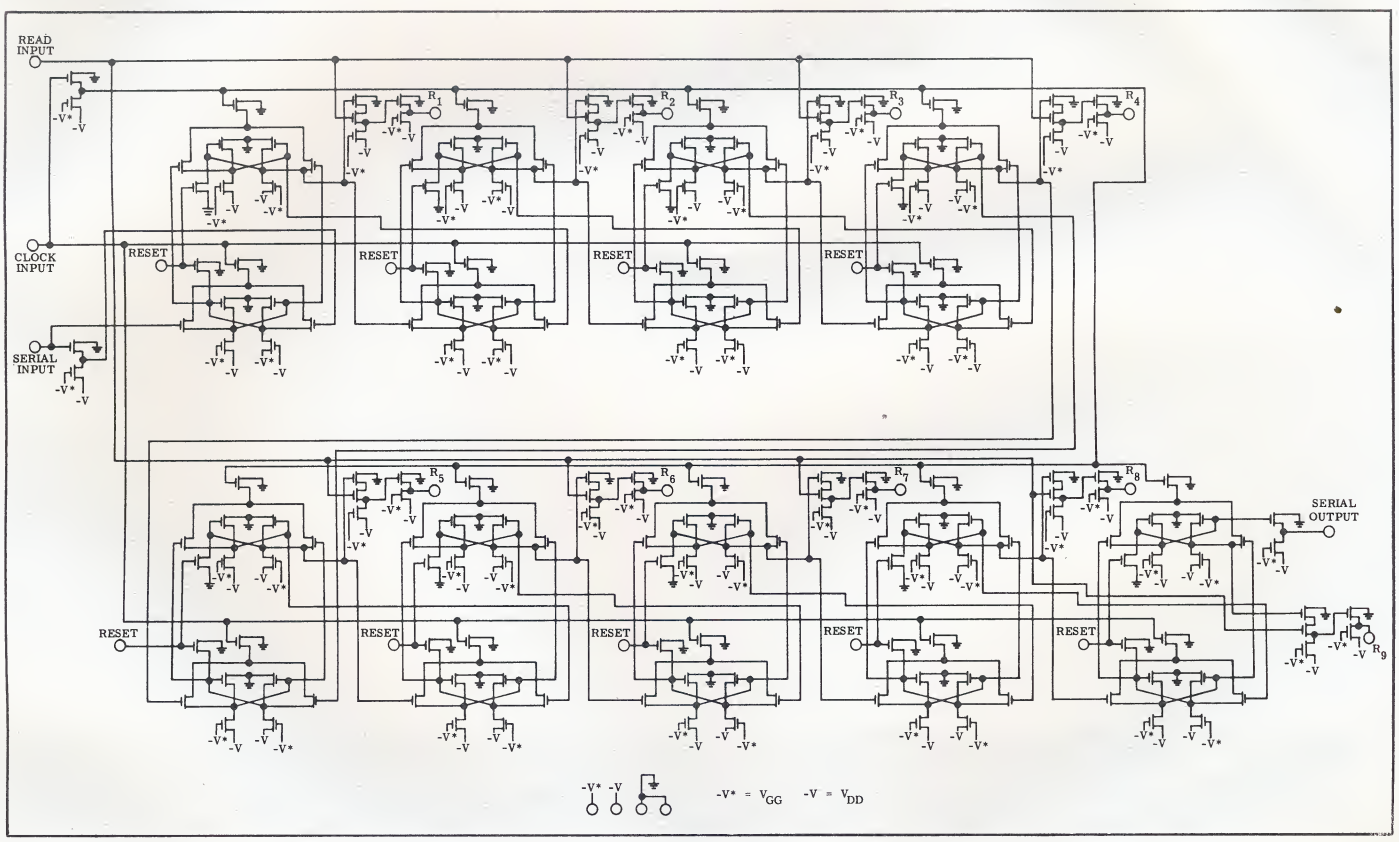
MAXIMUM RATINGS

Drain Voltage (V_{DD})	-30 v
Gate Voltage (V_{GG})	-30 v
Logic Input Voltages	-30 v
Storage Temperature	-55°C to +150°C
Operating Temperature Range (Note 5)	-55°C to +125°C
Power Dissipation T_A = 25°C	75 mw



SWITCHING-TIME CONSTANT DEFINITION

SCHEMATIC DIAGRAM



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9-BIT SHIFT REGISTER PARALLEL LOAD

pL 4R01

SEPTEMBER 1965

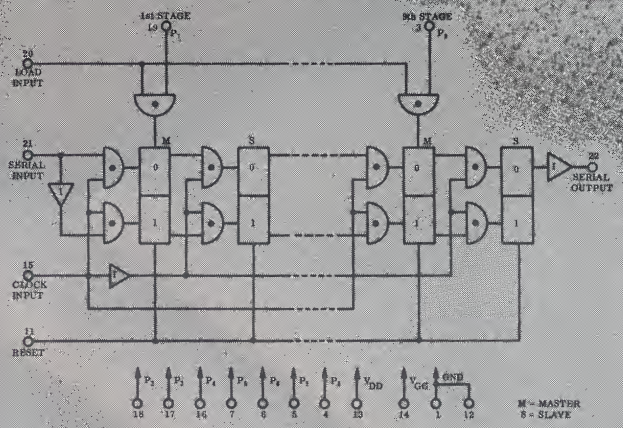
FUNCTION:

The GMe pL4R01, a monolithic integrated circuit using MOS devices, is a nine-stage shift register with inputs to each stage. This unit will operate from dc to 100 kc. The parallel inputs are gated by a "load" command which makes this unit useful as a parallel-to-serial converter. The pL4R01 is also useful as a delay element and temporary memory.

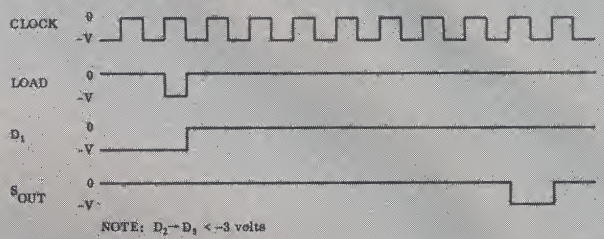
OPERATION:

The pL4R01 consists of nine master-slave flip-flops connected as a shift register. The master-slave flip-flops require a complete clock cycle to accomplish a one-bit shift. All inputs are buffered and inverted where necessary, requiring only single-line inputs. A negative clock signal (logic "1") shifts data into the master flip-flop and a ground signal (logic "0") shifts data from the master to the slave flip-flop. The reset and load commands are actuated by a logic "1" input. The reset signal is applied directly to both the master and slave flip-flops of all stages of the register. The ninth stage of the register has the true output available. It should be noted that the shift register should be parallel loaded only when the clock is at a logic "0." A typical operation of the pL4R01 is shown in the Timing Diagram.

FUNCTIONAL BLOCK DIAGRAM

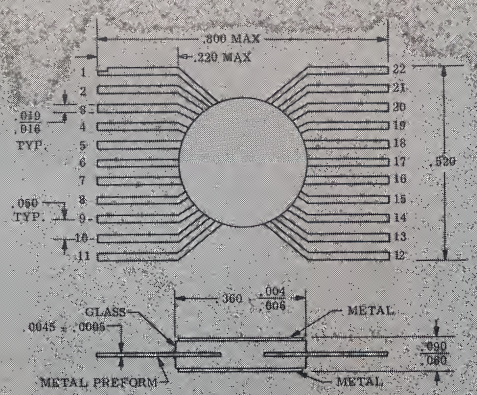


TYPICAL TIMING DIAGRAM



NOTE: $D_2 - D_9 < -3$ volts

PACKAGING



Pin No.	Description	Pin No.	Description
1	Ground	12	Ground
2	N.C.	13	Power Supply (V_{DD})
3	9th Preset Input (P_9)	14	Power Supply (V_{GG})
4	8th Preset Input (P_8)	15	Clock Input
5	7th Preset Input (P_7)	16	4th Preset Input (P_4)
6	6th Preset Input (P_6)	17	3rd Preset Input (P_3)
7	5th Preset Input (P_5)	18	2nd Preset Input (P_2)
8	N.C.	19	1st Preset Input (P_1)
9	N.C.	20	Load Input
10	N.C.	21	Serial Input (S_{IN})
11	Reset	22	Serial Output (S_{out})

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SEPTEMBER 1965

ELECTRICAL CHARACTERISTICS

T_A = -20°C to +70°C, V_{DD} = -12 v, V_{GG} = -24 v, Load = 10 MΩ and 7.5 pf

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock-Pulse Repetition Rate	dc		100	kc	Pulse Width = 5.0 μsec
Clock-Pulse Rise and Fall Time			10.0	μsec	Pulse Width = 100 μsec f = 1 kc
Input Pulse Width (Note 1)	1.0			μsec	
Input Logic Levels (Note 1)					
Logic "0" (V_{0TH})	0		-3.0	Volts	dc
Logic "1" (V_{1TH})	-9.0		-12.0	Volts	
Serial Output Logic Levels					
Logic "0" (V_{0TH})		-0.5	-2.0	Volts	dc
Logic "1" (V_{1TH})	-10.0	-11.0	-12	Volts	
DC Noise Immunity (Note 3)					
Logic "0" and Logic "1"	1.0			Volt	
Input Capacity		3.0		pf	V_{IN} = 0 v
Input Leakage Current			1.0	μa	V_{IN} = -10 v
Output Impedance to Ground (Output Logic "0")		1000	2000	Ohms	
Turn-off Time (T_{OFF}) (Note 2)		1.5	2.0	μsec	Input Logic Levels "0" = -2 v, "1" = -10 v
Turn-on Time (T_{ON}) (Note 2)		0.1	0.5	μsec	Input Logic Levels "0" = -2 v, "1" = -10 v

NOTES

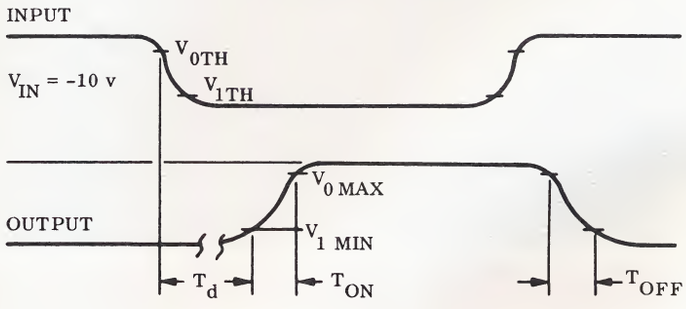
1. The input logic levels apply to serial input, load, nine preset inputs, reset, and clock input.
2. Turn-on and turn-off times are defined as logic level changes.
3. DC noise immunity is defined as follows:

$$\text{"1" State N.I.} = V_{1\,MIN} - V_{1\,TH} = |-10| - |-9| = 1\text{ v}$$
$$\text{"0" State N.I.} = V_{0\,TH} - V_{0\,MAX} = |-3| - |-2| = 1\text{ v}$$

4. Exercise caution to insure that the power supplies and input signals do not exceed +0.3 volts; otherwise, the PN junction used for gate protection will be forward-biased and damage may result.
5. Manufacturer reserves the right to make design and process improvements.
6. The bias voltages of V_{DD} = -12 v and V_{GG} = -24 v were selected for -20°C to +70°C operation.

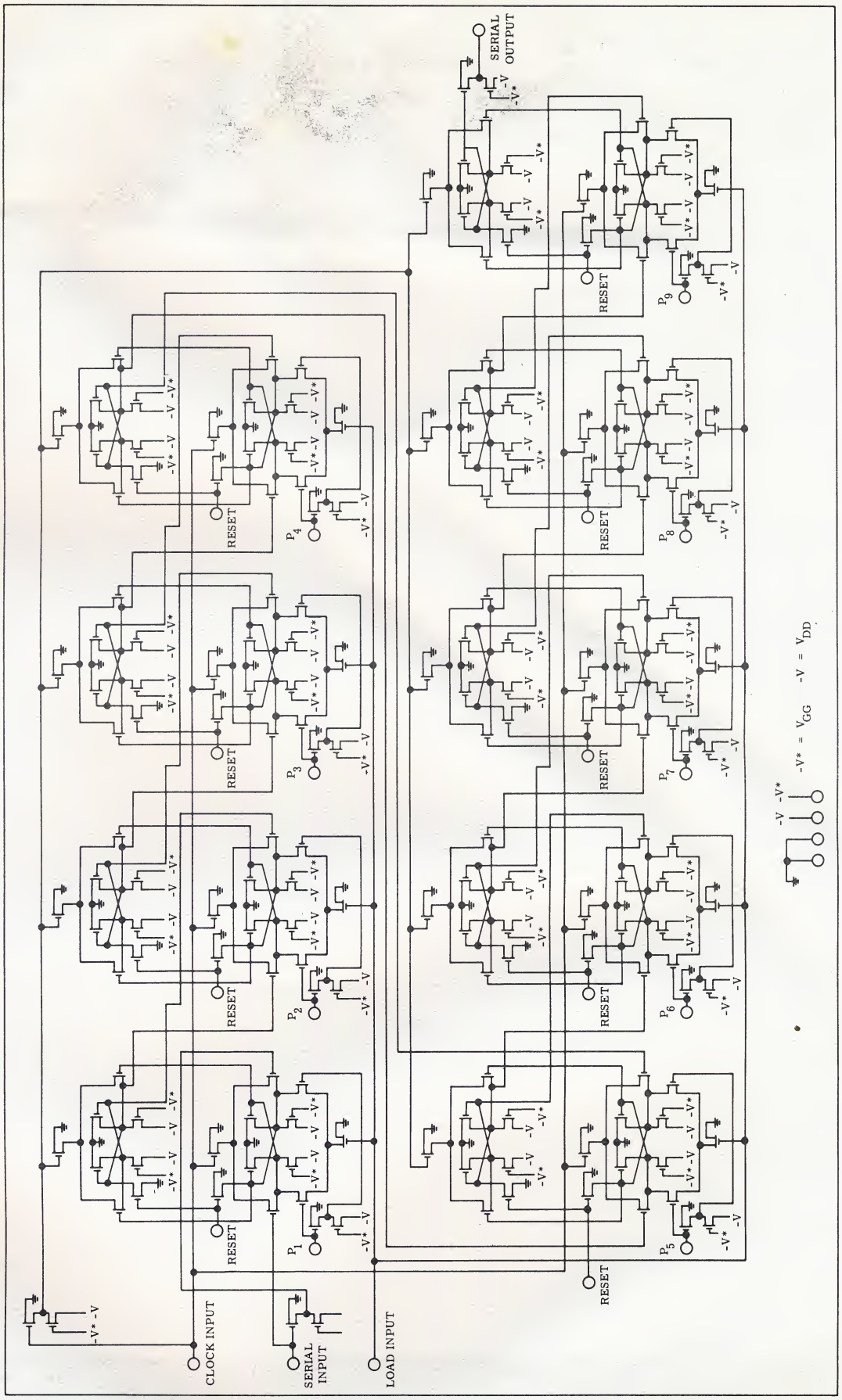
MAXIMUM RATINGS

Drain Voltage V_{DD}	-30 v
Gate Voltage V_{GG}	-30 v
Input Signal Voltages	-30 v
Storage Temperature	-55°C to +150°C
Operating Temperature Range (Note 6)	-55°C to +125°C
Power Dissipation T_A = 25°C	75 mw



SWITCHING-TIME CONSTANT DEFINITION

SCHEMATIC DIAGRAM



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